Remarks

The non-final Office Action dated November 25, 2008, notes the following: a suggestion to add section headings; a rejection of claims 3 and 5 under 35 U.S.C. § 112(2); a rejection of claims 1, 5 and 7 under 35 U.S.C. § 102(b) over Thuringer (U.S. Patent No. 6,498,404); a rejection of claims 2-4 under 35 U.S.C. § 103(a) over the '404 reference in view of the Patterson reference ("Computer Architecture: A Quantitative Approach"); and a rejection of claim 6 under 35 U.S.C. § 103(a) over the '404 reference. In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Regarding the Office Action's suggestions under 37 C.F.R. § 1.77(b), Applicant respectfully declines to add section headings. Such section headings are not statutorily required for filing a non-provisional patent application under 35 U.S.C. § 111(a). The guidelines at 37 C.F.R. § 1.51(d) are only suggestions for applicant's use and are not mandatory. When Rule 77 was amended in 1996, Bruce A. Lehman, Assistant Secretary of Commerce and Commissioner of Patents and Trademarks, stated in the Official Gazette: "Section 1.77 is permissive rather than mandatory. ... 1.77 merely expresses the Office's preference for the arrangement of the application elements. The Office may advise an applicant that the application does not comply with the format set forth in 1.77, and suggest this format for the applicant's consideration; however, the Office will not require any application to comply with the format set forth in 1.77." *See* 61 FR 42790, Aug. 19, 1996.

Applicant respectfully traverses the § 112(2) rejection of claims 3 and 5 because explicit antecedent basis is not required. *See, e.g.,* M.P.E.P. § 2173.05(e). Applicant submits that antecedent basis for the term the combinatorial circuits can be found in line 2 of claim 2 ("combinatorial logic circuits") and that antecedent basis for the term the electronic circuit can be found in line 1 of claim 1 ("an electronic circuit device"). Thus, claims 3 and 5 are definite. As such, the § 112(2) rejection of claims 3 and 5 is improper and Applicant requests that it be withdrawn. In an effort to facilitate prosecution, Applicant has amended claims 3 and 5 to provide explicit antecedent basis for the above discussed claim terms.

Applicant respectfully traverses the § 102(b) rejection of claims 1, 5 and 7 and the § 103(a) rejections of claims 2-4 and 6 because the cited portions of the '404 reference do not correspond to numerous aspects of the claimed invention. Applicant submits that the cited portions of the '404 reference do not teach or suggest an activity monitoring circuit that is coupled to receive pairs of processing signals coming into and out of respective ones of the processing circuits. For example, the '404 reference teaches that AND gate 8 (*i.e.,* the asserted activity monitoring circuit) only receives the complements of the signals input to AND gate 5 (*i.e.,* the asserted processing circuit), instead of receiving multiple pairs of processing signals from different respective processing circuits as in the claimed invention. *See, e.g.,* Figure 2, Col. 1:45-65, and Col. 2:39-54. The AND gate 8 also does not receive any processing signals coming out of AND gate 5. Moreover, since AND gate 8 only receives signals from a single processing circuit (*i.e.,* AND gate 5), AND gate 8 does not derive a combined activity signal indicative of a sum of power supply currents that are consumed by multiple processing circuits as does Applicant's activity monitoring circuit.

In addition, Applicant submits that the cited portions of the '404 reference do not teach or suggest a current drawing circuit that draws a cloaking current responsive to the combined activity signal produced by the activity monitoring circuit. The Office Action appears to be asserting that AND gate 8 also corresponds to Applicant's current drawing circuit. However, since AND gate 8 only receives signals from a single processing circuit, AND gate 8 does not draw a current responsive to the sum of power supply currents that are consumed by multiple processing circuits as does Applicant's current drawing circuit. Furthermore, Applicant submits that the Office Action's apparent assertion that AND gate 8 corresponds to both the activity monitoring circuit and the current drawing circuit of the claimed invention is illogical because a single element cannot correspond to Applicant's two separate elements, one of which is controlled responsive to a signal produced by the other.

In view of the above, the cited portions of the '404 reference do not correspond to numerous aspects of the claimed invention. Accordingly, the § 102(b) rejection of claims 1, 5 and 7 and the § 103(a) rejections of claims 2-4 and 6 are improper and Applicant requests that they be withdrawn.

In the event that the Examiner is asserting that some other (unidentified) component of the '404 reference allegedly corresponds to Applicant's activity monitoring circuit and/or Applicant's current drawing circuit, Applicant respectfully requests clarification. In order to comply with 35 U.S.C. § 132, sufficient detail must be provided by the Examiner regarding the alleged correspondence between the claimed invention and the cited reference to enable Applicant to adequately respond to the rejections. *See, also,* 37 C.F.R. § 1.104 ("The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.") and M.P.E.P. § 706.02(j), ("It is important for an Examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply."). Applicant should also be afforded an opportunity to respond to such clarification prior to a final rejection. *See, e.g.,* M.P.E.P. § 706.07 ("Before final rejection is in order a clear issue should be developed between the examiner and applicant.").

Applicant has added new claims 8-14, which depend from either claim 1 or claim 7. As such, Applicant submits that claims 8-14 are allowable over the cited references for at least the reasons discussed above. Applicant notes that support for claims 8-14 can be found throughout Applicant's disclosure including, for example, in Figure 1 and the related discussion in Applicant's specification.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-9063 (or the undersigned).

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